Zynq SoC 설계

VHDL/Verilog HLS(SDSoC)

Xilinx VIVADO

AXI HW IP



Zynq를 활용한 SoC / FPGA 설계

HDL 및 HLS를 이용한 설계 이해 및 실습



ZYNQ를 이용한 설계 실습(HDL)

CONTENTS01. Vivado Tutorial02. Processing System Tutorial03. S/W & H/W Co-Design Tutorial



Vivado

- Xilinx에서 개발한 개발 도구
- ISE 대체
- 7-Series 부터 지원(Spartan7, Artix7, Kintex7, Virtex7, Zynq7000)
- IP 재사용(IP Integrator → 사용, 관리, 생성) 디자인
- GUI 기반 블록 디자인

ISE – Vivado 주요 차이점

	ISE	Vivado
Simulator	ISIM	XSIM
Debug	Chipscope analyzer	Vivado(Integrated Chipscope)
Design	RTL + XPS	RTL + Block Design





Vivado 다운로드/설치

자일링스 홈페이지 (www.Xilinx.com)에서 Vivado 설치 파일을 다운로드 받는다.

Vivado Design Suite - HLx Editions - 2018.2 Full Product Installation

Important	Download Includes	Vivado Design Suite HL Editions (All Editions)
We strongly recommend to use the web installers as it reduces download	Download Type	Full Product Installation
time and saves significant disk space.	Last Updated	Jun 18, 2018
Please see Installer Information for details.	Answers	2018.x - Vivado Known Issues
Microsoft Internet Explorer web bowsers.	Documentation	Release Notes
	Enablement	License Solution Center
Vivado HLx 2018.2: WebPACK and Editions - Windows Self Extracting Web Installer (EXE - 50.56 MB)		
MD5 SUM Value : 1b00a58303ddb3bca5e84fa1b26685b0		
▲ Vivado HLx 2018.2: WebPACK and Editions - Linux Self Extracting Web		
Installer (BIN - 99.45 MB)		
MD5 SUM Value : 982490570f0c379bfcdeb32a31a5d0af		
Download Verification 😯		
Digests Signature Public Key		
Vivado HLx 2018.2: All OS installer Single-File Download (TAR/GZIP - 17.11 GB)		
MD5 SUM Value : e878f870bb9d1dfc882b005550cfdbef		
Download Verification 🕜		
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Vivado 다운로드/설치

WebPack 에디션 설치 SDK 및 SoC Device, Cable Driver 선택 및 설치



Vivado Tutorial

- 일반적인 FPGA 프로젝트(ISE)
 - 프로젝트 계획 수립
 - 소스코드 생성
 - 시뮬레이션
 - 합성 / 구현
 - 타이밍 시뮬레이션
 - BIT 파일 생성





Design Description

• 스위치 입력에 따라 0-255 카운터 값 LED에 출력





- Vivado를 실행하여 프로젝트를 생성 한다.
- File Project New
- Quick Start Create Project 실행





💫 New Project	×
Project Name Enter a name for your project and specify a directory where the project data files will be stored.	4
Project name: utorial Project location: C:/work/23_workplace Create project subdirectory Project will be created at: C:/work/23_workplace/tutorial	2
? < <u>Back</u> <u>Next</u> ≥ <u>Finish</u> Cance	I





프로젝트 타입 지정 → RTL HUINS



default Language 선택

12

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사용 FPGA/SoC 파트 선택 ()xc7z020clg484-1 Н Human Intelligent System







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Settings				,		,					
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Language Templates	> Constraints	3		Pr	oject na	me:	t	utorial			
₽ IP Catalog	~ 🚍 Simulation	Project location: C:/			:/work/23_workplace/tutorial						
	🗅 sim_1	Product family: Zyn			lynq-7000						
Y IP INTEGRATOR	Hierarchy Lib	raries Com	pile Order	Pr	Project part: xc7			:7z010clg225-1			
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	Add or create <u>simulation sources</u>
E XILINX.	
?	< <u>B</u> ack <u>Einish</u> Cancel

Constraints → Timing, Clock, Pin map Design Source → HDL, Block Design, IP Simulation → Test Bench



Add Sources Add or Create Design Sources Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.	. Create Source File
Luse Add Files, Add Directories or Create File buttons below Add Files Add Directories Create File Scan and add RTL include files into project Copy gources into project Add sources from subdirectories	Create a new source file and add it to your project. Eile type: Verilog File name: Verilog Header File location: System/Verilog VHDL Memory File

Add → 파일, 디렉토리 추가

Create File → 소스 파일 생성(counter255.v) Copy Sources into project → 소스코드 사본 추가



15



모듈 이름 및 I/O 설정

- input: SW, Reset
- output: [7:0] LED

미 설정시 빈 모듈 생성

🝌 Def	L Define Module								×	
Def For M P	Define a module and specify I/O Ports to add to your source file. For each port specified: MSB and LSB values will be ignored unless its Bus column is checked. Ports with blank names will not be written.									
Мо	Module Definition									
	<u>E</u> ntity name:		count	er255				\otimes		
	Architecture n	ame:	Beha	vioral				\otimes		
	I/O Port Definitions									
	+ -	1	Ψ.							
	Port Name	Dire	ction	Bus	MSB	LSB				
	SW	in	~		0	0				
	Reset	in	~		0	0				
	LED	out	~	<	7	0				
?	OK Cancel									

ΗU

소스 코드 작성(counter)

스위치 입력 시(posedge) - 레지스터 값(LED) 1 증가 리셋 입력 시(Negative Reset) - 0으로 초기화

0-255 값 LED 출력

Project Summary × counter255.v ×							
C:/work/10_SDx/tutorial/tutorial.srcs/sources_1/new/counter255.v							
Q 🖮 ★ ≁ X 🗉 🖬 X // 🎟 ♀							
1 `timescale ins / ips							
2 由 ///////////////////////////////////							
21							
22							
23 🖨 module counter255(
24 : input SW.							
25 input Reset							
26 output reg [7:0] LED							
27):							
28 '							
20 j 29 j always@(nosedge_SW) begin							
20 d (IPoset)							
21 ' LED Z= 0'							
34 — ena							
36 ⊖ endmodule							



RTL Analysis

RTL ANALYSIS – Schematic

RTL 소스 코드 → Schematic 표현

REG 값 LED 출력 SW 입력시 1 ADD Reset 시 초기화

_ **D** _ X 👃 tutorial - [C:/work/10_SDx/tutorial/tutorial.xpr] - Vivado 201 Window Layout View Help Q- Quick Access File Edit Flow Tools Reports Readv ▶ 0 0 × 👁 🕨 👭 🛱 🖸 🌞 Σ 1/2 D X 🔡 I/O Planning E, ~ Flow Navigator ELABORATED DESIGN - xc7z020clq484-1 (active) **₹ ≑ ?** ? X PROJECT MANAGER Sources Netlist Device Constraints x Device x counter255.v x Schematic ? _ 🗆 🖸 ? 🗆 🗹 Settings ÷. Q 🛨 🌲 🗕 ø Add Sources Internal VREF Language Templates 📄 0.6V P IP Catalog 📄 0.675V 0.75V IP INTEGRATOR LED i 🕞 0.9V V > NONE (4) S=1"b0 I0 Create Block Design 0 I/O Bank 13 S=default 11 Open Block Design RTL MUX Generate Block Design Drop I/O banks on voltages or the "NONE" folder to set/unset Internal VREF Reset LED reg[7:0] RST ✓ SIMULATION sw 🗋 -D LED[7:0] Source File Properties × Clock Regions ? _ 🗆 🖸 0 Run Simulation LED0_i D 11 counter255.v ← | ⇒ | ✿ O[7:0] 10[7:0] RTL REG SYNC RTL ANALYSIS Enabled RTL ADD Open Elaborated Design C:/work/10 SDx/tutorial/tutorial.srcs/sources 1/ner Location 🖄 Report Methodology Verilog Type: Report DRC < General Properties Report Noise Schematic Messages Log Reports Design Runs Package Pins I/O Ports **Tcl Console** ? _ 🗆 🖸 4 + 뇌 ø Q, Ŧ ۲ SYNTHESIS Direction Neg Diff ... Package Pin Fi... B... I/O Std Drive Strength Slew Type Pull Type Name Vcco Run Synthesis All ports (10) > Open Synthesized Design > 🕤 LED (8) OUT default (LVCMOS18) v 1.800 12 SLOW NONE 6 > Scalar ports (2) IMPLEMENTATION Run Implementation > Open Implemented Design

I/O Planning

Package 탭 I/O의 핀 맵핑 설정

T16	LED[7]	LVCMOS3.3V
T17	LED[6]	LVCMOS3.3V
R19	LED[5]	LVCMOS3.3V
T19	LED[4]	LVCMOS3.3V
R18	LED[3]	LVCMOS3.3V
T18	LED[2]	LVCMOS3.3V
P16	LED[1]	LVCMOS3.3V
R16	LED[0]	LVCMOS3.3V
AA18	SW	LVCMOS3.3V
Y18	Reset	LVCMOS3.3V

tutorial - [C:/work/10_SDx/tutorial/tutorial.xpr] - Vivado 2018.3	
Eile Edit Flow Tools Reports Window Layout View Help Q- Quick Access	Ready
	📰 I/O Planning 🛛 🗸
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PROJECT MANAGER	2 0 17
Settings	* • • •
Add Sources	×
Language Templates	
Create Block Design	
Open Block Design	
Generate Block Design Drop I/O banks on voltages or the "NONE" folder to set/unset Internal VREF.	
Run Simulation Source File Properties × Clock Regions ? _ Clock Re	
$ \bigcirc \text{ counter255.v} \qquad \leftarrow \Rightarrow \diamond \qquad R \qquad \qquad \bullet \qquad$	
Open Elaborated Design Location: Chwork/10. SDythutorial brocksources. The W	
Report DRC	
Report Noise General Properties	
A Schematic	
TCI Console Messages Log Reports Design Runs Package Pins VO Ports X	? _ 🗆 🖒
Y SYNTHESIS	۵
Run Synthesis Name Direction Neg Diff Package Pin Fi B VO Std Vcco Drive Strength Slew Type	Pull Type
> Open Synthesized Design	
✓ 1 LED (8) OUT Operating (LVCMOS18) ▼ 1.800 12 ✓ SLOW ✓ ✓ 1 E OUT ✓ Idefault (LVCMOS18) ▼ 1.800 12 ✓ SLOW ✓	
INPLEMENTATION ILE OUT V default (LVCMOS18) 1800 12 V SLOW	
Run Implementation ☐ LE OUT ✓ default (LVCMOS18) ▼ 1.800 12 ✓ SLOW	V NONE V
> Open Implemented Design	V NONE V
	> [×]

Constraints

저장 시 constraints 생성

Add Sources → xdc 파일 생성, 추가 또한 가능

Save Constraints								
Select a target file to write new unsaved constraints to. Choosing an existing file will update that file with the new constraints.								
• <u>C</u> reate a new file								
<u>F</u> ile type:	XDC	~						
F <u>i</u> le name:	top.xdc	\otimes						
Fil <u>e</u> location:	📮 <local project="" to=""></local>	~						
Select an existing fil	e							
<select a="" targ<="" td=""><td>jet file></td><td>~</td></select>	jet file>	~						
?	ок	Cancel						

21 22 **set**

top.	xdc × counter255.v ×
C:/v	vork/10_SDx/tutorial/tutorial.srcs/constrs_1/new/top.xdc
Q,	
1	<pre>set_property PACKAGE_PIN T16 [get_ports {LED[7]}]</pre>
2	<pre>set_property PACKAGE_PIN T17 [get_ports {LED[6]}]</pre>
3	<pre>set_property PACKAGE_PIN R19 [get_ports {LED[5]}]</pre>
4	<pre>set_property PACKAGE_PIN T19 [get_ports {LED[4]}]</pre>
5	<pre>set_property PACKAGE_PIN R18 [get_ports {LED[3]}]</pre>
6	<pre>set_property PACKAGE_PIN T18 [get_ports {LED[2]}]</pre>
7	<pre>set_property PACKAGE_PIN P16 [get_ports {LED[1]}]</pre>
8	<pre>set_property PACKAGE_PIN R16 (get_ports {LED[0]})</pre>
9	<pre>set_property PACKAGE_PIN V18 [get_ports Reset]</pre>
10	<pre>set_property PACKAGE_PIN AA18 [get_ports SW]</pre>
11	<pre>set_property IOSTANDARD LVCMOS33 [get_ports {LED[7]}]</pre>
12	<pre>set_property IOSTANDARD LVCMOS33 [get_ports {LED[6]}]</pre>
13	<pre>set_property IOSTANDARD LVCMOS33 [get_ports {LED[5]}]</pre>
14	<pre>set_property IOSTANDARD LVCMOS33 [get_ports {LED[4]}]</pre>
15	<pre>set_property IOSTANDARD LVCMOS33 [get_ports {LED[3]}]</pre>
16	<pre>set_property IOSTANDARD LVCMOS33 [get_ports {LED[2]}]</pre>
17	<pre>set_property IOSTANDARD LVCMOS33 [get_ports {LED[1]}]</pre>
18	<pre>set_property IOSTANDARD LVCMOS33 [get_ports {LED[0]}]</pre>
19	<pre>set_property IOSTANDARD LVCMOS33 [get_ports Reset]</pre>
20	set property IOSTANDARD LVCMOS33 [get ports SW]

_property CLOCK_DEDICATED_ROUTE FALSE

SW 입력이 외부 클럭과 같이 작동하므로 내용 추가 set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets SW]



Simulation

Add Sources

- Simulation Sources
- 시뮬레이션 소스 추가



Simulation

시뮬레이션 소스 생성

File type: Verilog File name: tb_tutorial

💫 Add Sources	
Add or Create Simulation Sources	
Specify simulation specific HDL files, or directories of new source file on disk and add it to your project	A Create Source File
Specify simulation set: 🔚 sim 1	Create a new source file and add it to your project.
$ +_{j} = + + $	Eile type: Verilog 🗸
	F <u>i</u> le name: tb_tutorial 🛞
Line Add Films Add Dired	Fil <u>e</u> location: 🖕 <local project="" to=""> 🗸</local>
Use Add Flies, Add Dired	Сапсеl
Add Files Add	I Directories <u>C</u> reate File
Scan and add RTL include files into project	
✓ Copy sources into project	
\checkmark Add so <u>u</u> rces from subdirectories	
\checkmark Include all design sources for simulation	
? < <u>B</u> a	ck Next > Finish Cancel

System

Simulation Source

시뮬레이션 소스코드 작성

SW 입력 0, 1 toggle(clk) Reset = 0 일 때 0으로 초기화 LED 값 출력

```
"timescale ins / ips
21
22
23 🖯
      module tb_tutorial();
24
      reg SW, Reset;
25
26
      wire [7:0] LED:
27
28
      counter255 inst_counter255(SW, Reset, LED);
29
30 🖨
      initial begin
      S₩ = 0;
31
      forever #5 SW=~SW; //SW Toggle
32
33 Á
      end
34
      initial begin
35 E
      Reset=0;
36
37
      #20;
      Reset=1:
38
39
      #100;
      Reset=0:
40
      #20:
41
      Reset=1;
42
43 🖨
      end
      endmodule
44
```

Simulation

SIMULATION -Run Behavioral Simulation

시뮬레이션을 실행한다



Simulation Window

➡ Run All(end 까지 출력)



Simulation 출력 파형 확인



표기(16진수, 10진수), 색상 등 변경

26

 Run All 클릭 시 추가 시뮬레이션

 0 - 255 카운터

Simulation 출력 파형 확인

tb_tutorial.vhd × Untitled 1* × counter255.vhd ×

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신호를 아날로그 형태로도 출력할 수 있음



Synthesis – 합성

SYNTHESIS -Run Synthesis 실행

Schematic → 넷 리스트로 변환

Lutorial - [C:/work/23_workplace/tutorial/t	utorial.xpr] - Vivado 2018.2		
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Flow Navigator 😤 🚔 ?	PROJECT MANAGER - tutorial		? ×
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V IP INTEGRATOR	Q X \$ + ? ● 0	C:/work/23_workplace/tutorial/tutorial.srcs/sources_1/new/counter255.v	×
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Open Block Design	counter255 (counter255.v)	1 timescale ins / ips	^ =
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	top.xdc (target) Simulation Sources (1)	Launch the selected synthesis or implementation runs.	
Run Simulation	Hierarchy Libraries Compile Orde	/ · · · · · · · · · · · · · · · · · · ·	
✓ RTL ANALYSIS	Source File Properties ? _ C	Launch directory: 😱 <default directory="" launch=""></default>	
✓ Open Elaborated Design	🔵 counter255.v 🔶 🗕	Options	
Report Methodology	useu m	● Launch runs on local host. Number of jobs: 8 v	
Report DRC	✓ Synthesis	Generate scripts only	
Schematic	Implementation		
✓ SYNTHESIS	Simulation	Don't show this dialog again	
 <u>Run Synthesis</u> Open Synthesized Design 	General Properties	OK Cancel	×
	Tcl Console 🗙 Messages Log F	Reports Design Runs	? _ 🗆 🖒
IMPLEMENTATION Run Implementation	Q, X, ♦ II 🗈 🎟 🏛		
Open Implemented Design	irunali ⊨ close sim		^
. open implemented boolgit	☐ INFO: [Simtcl 6-16] Simulation clos	sed (
Y PROGRAM AND DEBUG	close_design		
👫 Generate Bitstream			> ``
> Open Hardware Manager	Type a Tcl command here		
Run synthesis on your project source files			



Schematic 창 - LUT, FF으로 구현 - 입력, 출력 버퍼 - I/O 포트(LED, SW)



Н



Project Summary에서 사용된 리소스 정보 확인

- LUT
- FF
- 10

- BUFG

Project Summary	? □ 岱 >	ζ
Overview Dashboard		
		^
Synthesis	Implementation	
Status:CompleteMessages:1 warningPart:xc7z020clg484-1Strategy:Vivado Synthesis DefaultsReport Strategy:Vivado Synthesis Default Reports	Status:Not startedMessages:No errors or warningsPart:xc7z020clg484-1Strategy:Vivado Implementation DefaultsReport Strategy:Vivado Implementation Default ReportsIncremental implementation:None	
DRC Violations	Timing	l
Run Implementation to see DRC results	Run Implementation to see timing results	l
Utilization Post-Synthesis Post-Implementation	Utilization Post-Synthesis Post-Implementation	
Graph Table	Graph Table	
LUT - 1%	Resource Estimation Available Utilization %	l
FF 1 1% IO - 5%	LUT 7 53200 0.01	l
BUFG - 3%	FF 8 106400 0.01	
0 25 50 75 100	IO 10 200 5.00	
Estimated Utilization (%)	BUFG 1 32 3.13	

Implementation

Xilinx FPGA Implementation

- Translate Netlist Translate(NGC → NGD)
- Map Netlist 해당 장치 리소스 매핑 LUT, FF, BRAM
- Place & Route 실제 FPGA 리소스 연결, 배치



Implementation

Netlist의 연결, 배치 확인

LED_OBUF 선택 시 SLICE X1Y1에 배치된 것 확인 가능

SW \rightarrow SW_IBUF SLICE(LUT \rightarrow REG) REG \rightarrow LED_OBUF \rightarrow PAD



Implementation

Project Summary

- 1. 실제로 배치에 사용된 리소스
- 2. 타이밍 정보
- 3. 예상 소모 전력

roject Summary × top.xdc ×		? 🗆 🖸
Synthesis	Implementation	Summary Route Status
Status: ✓ Complete Messages: • 1 warning Part: xc7z010cig225-1 Strategy: Vivado Synthesis Defaults Report Strategy: Vivado Synthesis Default Reports	Status: Complete Messages: 6 warnings Part: xc7z010clg225-1 Strategy: Vivado Implementation Defaults Report Strategy: Vivado Implementation Default Reports Incremental compile: None	
DRC Violations	Timing	Setup Hold Pulse Width
Summary: 0 2 warnings Implemented DRC Report	Worst Negative Slack (WNS): NA Total Negative Slack (TNS): NA Number of Failing Endpoints: NA Total Number of Endpoints: NA Implemented Timing Report Implemented Timing Report	2
tilization Post-Synthesis Post-Implementation Graph Table LUT 1 1% FFF 1 1% 0 25 50 75 100 Utilization (%) 1	94% Dynamic: 11.795 W (94%) 94% Signals: 0.100 W (1%) 98% Logic: 0.077 W (1%) 90: 11.617 W (98%) 6% Dome	Summary On-Chip
		HUI

Bit 파일 생성

PROGRAM AND DEBUG – Generate Bitstream

FPGA에 다운로드 할 Bitstream 파일을 생성한다.

<u>F</u> ile <u>E</u> dit F <u>l</u> ow <u>T</u> ools Rep	o <u>o</u> rts <u>W</u> indow La <u>v</u> out <u>V</u> iew <u>H</u> elp	Q- Quick Access			Impler	mentation Comp	olete ,
	▶ I≣ ✿ ∑ ∞ ∞ ×				∷ De	ault Layout	~
Flow Navigator 🛛 😤 🌲 ? 💷	PROJECT MANAGER - tutorial						?
Y PROJECT MANAGER	Sources ? _ □ Ľ X	Project Summary × top	p.v × t	op.xdc ×		?	0 6
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PC에 보드 연결

JTAG 케이블로 PC와 연결

Hardware Manager

- Open New Target 실행
- Local Server로 연결

Auto Connect 실행 시 자동으로 연결





PC에 보드 연결

JTAG 케이블로 PC와 연결

Hardware Manager

- Open New Target 실행
- Local Server로 연결

Auto Connect 실행 시 자동으로 연결





elect local or re ettings. Use Lo	emote hardware server, then configure the host name and port P
<u>C</u> onnect to:	Local server (target is on local machine)
Click Next to local machin	aunch and/or connect to the hw_server (port 3121) application on the e.

Human Intelligent
PC에 보드 연결

natuwate <u>t</u> ary	ets					
Туре	Name		JTAG Clock F	requency		
xilinx_tcf	Xilinx/Port_#0004	4.Hub_#0006	6000000	× .		
			Add Xilinx Virtu	al Cable (XV	2)	
Hardware <u>D</u> evio	ces (for unknown	devices, spec	Add Xilinx Virtua	al Cable (XV ion Register	C) (IR) length)	
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Hardware <u>D</u> evio Name @ arm_dap_(ces (for unknown ID Code 4BA00477	devices, spec IR Length 4	Add Xilinx Virtua	al Cable (XV ion Register	C) (IR) length)	

여러 디바이스 연결 시 Hardware Devices 정보 확인 후 선택 Part: xc7z020_1

JTAG Clock 설정 후 연결



Program Device

HARDWARE MANAGER - localhost/xilinx_tcf/	Xilinx/Port_#0004.Hub_#0006
() There are no debug cores. Program dev	vice Refresh device
Hardware	? _ O Ľ X
Q ¥ \$ \$ ▶ ≫ ■	•
Name	Status
V 🛽 localhost (1)	Connected
✓ ■	Open
arm_dap_0 (0)	N/A
✓ ⊕ xc7z020_1 (1)	Hardware Device Properties
1 XADC (System Monite	
	Program Device
	Verify Device
c	Refresh Device
<	Add Configuration Memory Device
	Boot from Configuration Memory Device
Hardware Device Properties	Program BBR Key
<pre>@ xc7z020_1</pre>	Clear BBR Key

Bit 파일 선택 후 FPGA에 다운로드







스위치(SW1)을 누른 상태에서(Reset=0) S2를 입력 시(Posedge SW) 0으로 초기화

스위치(SW2) 입력 시 LED 출력이 1씩 증가





Vivado Tutorial Summary

- Vivado 통한 HDL Design Flow
- 프로젝트 생성 HDL 소스 작성
- 시뮬레이션을 통한 작동 테스트
- Synthesize → Implement → Bit 파일 생성



2. Processing System Tutorial

Vivado

- A. 프로젝트 생성
- B. Processing System 설정
 - I/O Peripheral(UART)
 - DDR3 Memory Controller
 - HW Export

SDK

- C. 애플리케이션 프로젝트 생성
- D. "Hello World" 출력



Zynq Processing System

APU

- ARM Cortex-A9
- L2 Cache
- OCM(On Chip Memory)

I/O Peripherals - MIO(PS), EMIO(PL) DRAM Controller





Vivado를 실행하여 프로젝트를 생성한다.

File → Project → New 또는 Quick Start → Create Project





🚴 New Project		×
Project Name Enter a name for yo	ur project and specify a directory where the project data files will be stored.	4
<u>P</u> roject name:	zynq_tutorial	8
Project location:	C:/work/23_workplace	⊗
🖌 Create projec	t subdirectory	
Project will be cro	eated at: C:/work/23_workplace/zynq_tutorial	
(?)	< <u>B</u> ack <u>Next</u> > <u>F</u> inish	Cancel

프로젝트 이름, 경로 지정

You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis,

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and

Do not specify design sources. You will be able to view part/package resources.

Create a Vivado project from a Synplify, XST or ISE Project File.

Create a new Vivado project from a predefined template.

📐 New Project

Project Type

<u>RTL Project</u>

Specify the type of project to create.

implementation.

I/O Planning Project

Imported Project

Example Project

implementation, design planning and analysis.

<u>D</u>o not specify sources at this time

Do not specify sources at this time

x



+, - +		Parts	Boards							
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Add so <u>u</u> rces from subdire	tories	xc7z02	0clg484-1	484	200	53200	1	06400	140	0
arget language: Verilog	✓ Simulator language: Mixed ✓	<		•						
VIII DE										

사용 FPGA/SoC 파트 선택 ()xc7z020clg484-1 Н Human Intelligent System

소스 수거(파걸, 놀니, 생성) default Language 선택

Processing System IP 추가

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Run Implementation													
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Create and add an IP subsystem to the proj	ect			_									,





Zynq PS IP 추가



B. Processing System 설정

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	processing_system7_0	
	DDR + FIXED_IO + M_AXI_GP0_ACLK ZYNQ. M_AXI_GP0 + FCLK_CLK0 FCLK_RESET0_N	
	ZYNQ7 Processing System	

Zynq PS 설정

- I/O Peripheral \rightarrow UART
- Memory Controller
- 32b GP AXI Master





B. Processing System 설정

Documentation 🔹 Pres	ets 📄 IP Location 🔅 Impo	ort XPS Settings					
Page Navigator —	MIO Configuration					Sum	mary Report
ynq Block Design	Bank 0 I/O Voltage LVCMO	NS 3.3V 🗸	Bank 1 I/O Voltage	EVCMOS 3.3V 🗸			
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eripheral I/O Pins	Search: Q-						
IIO Configuration	Peripheral	ю	Signal	Ю Туре	Speed	Pullup	Direction
	✓ I/O Peripherals						
Clock Configuration	>						
DR Configuration	>						
-	USB 0						
MC Timing Calculation	USB 1						
terrupts	> 🗌 SD 0						
	> 🗌 SD 1						
	> UART 0						
	> 🗹 UART 1	MIO 48 49	~				
	L 12C 0						
	🗌 I2C 1						
	> 🗌 SPI 0						
	> SPI 1						



UART1을 Enable 하며, MIO 48-49번 핀 할당

DRAM Controller의 값을 변경한다 (다음 페이지 표 참조)



Documentation 🔅 Pres	ets 🔚 IP Location 🔅 Import XPS Setting	gs		Occur
Page Navigator —	DDR Configuration		Summary Report	Page
Zynq Block Design	Enable DDR			Zynq Bl
PS-PL Configuration	← Q <u></u>			PS-PL
Peripheral I/O Pins	Search: Q-			Periphe
MIO Configuration	Name	Select	Description	MIO Co
	 DDR Controller Configuration 		î l	Ob at 6
Clock Configuration	Memory Type	DDR 3 🗸 🗸	Type of memory interface. Refer to UG585 Zyng Technical Reference	Clock
DDR Configuration	Memory Part	MT41J256M16 R 🗸	Memory component part number. For unlisted parts choose "Custon	DDR C
	Effective DRAM Bus Width	MT41J128M16 HA-187E	width of DDR interface, not including ECC data width. Refer to U	
SMC TIMING Calculation	ECC	MT41J512M8 RA-15E	es error correction code support. ECC is supported only for an	SMCT
Interrupts	Burst Length	MT41K128M16 HA-15E	um number of data beats the controller should use when com	Interru
	DDR	MT41K256M16 RE-125	ory clock frequency. The allowed freq range is (200.000000 : 53	
	Internal Vref		Enables internal voltage reference source. Disable to use external V	
	Juntion Temperature (C)	MT41K256M8 DA-15E	led operating temperature range. Controls the DDR refresh inti	
	> Memory Part Configuration	MT41K256M8 HX-15E		
	 Training/Board Details 	MT41J256M16 RE-125		
	> DRAM Training	Custom	~	
	 DQS to Clock Delay (ns) 		~ · · · · · · · · · · · · · · · · · · ·	

Documentation 🔅 Pres	ets 🛯 📄 IP Location 🔅 Import XPS S	ettings		
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Zynq Block Design	Enable DDR			
PS-PL Configuration	← Q 풒 ≑			
Peripheral I/O Pins	Search: Q-			
	Name	Select		Description
MIC Configuration	> DRAM Training			
Clock Configuration	 DQS to Clock Delay (ns) 			
DDR Configuration	DQS0	0.171	8	DQS to Clock delay [0] (ns). The DQS path delay subtracted from
g	DQS1	0.172	⊗	DQS to Clock delay [1] (ns). The DQS path delay subtracted from
SMC Timing Calculation	DQS2	0.168	8	DQS to Clock delay [2] (ns). The DQS path delay subtracted from
Interrupts	DQS3	0.118	8	DQS to Clock delay [3] (ns). The DQS path delay subtracted from
	✓ Board Delay (ns)			
	DQ[7:0]	0.333	8	Board delay [0] (ns). The midrange of data (DDR_DQ, DDR_DM)
	DQ[15:8]	0.334	8	Board delay [1] (ns). The midrange of data (DDR_DQ, DDR_DM)
	DQ[23:16]	0.346	8	Board delay [2] (ns). The midrange of data (DDR_DQ, DDR_DM)
	DQ[31:24]	0.358	8	Board delay [3] (ns). The midrange of data (DDR_DQ, DDR_DM)
	Additive Leteney (gyelen)	0		Additive Latency (cycles) Increases the officiency of the common

B. Processing System 설정

📐 Re-customize IP

B. Processing System 설정

[표] Memory 설정 내용

7	방 목	내용	항목	<u>t</u>	내용
Memo	ry Type	DDR3		DQS0	0.171
Memo	ory Part	MT41J256M 16 RE-125	DQS to Clock	DQS1	0.172
Interr	nal Vref	Check	Delay (ns)	DQS2	0.168
DDAM	Write leveling	Check		DQS3	0.118
DRAM	Read gate	Check		DQ[7:0]	0.333
Training	Read data eye	Check	Board Delay	DQ[15:8]	0.334
			(ns)	DQ[23:16]	0.346
				DQ[31:24]	0.358

HUINS

B. Processing System 설정

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$\mathbf{Q} \mid \mathbf{Q} \mid \mathbf{X} \mid \mathbf{X} \mid \mathbf{O} \mid \mathbf{Q} \mid \mathbf{X} \mid \mathbf{X} \mid \mathbf{Q} \mid \mathbf{X} \mid \mathbf{X} \mid \mathbf{Q} \mid \mathbf{X} \mid $	🖌 🖸 🖈 C 🗿 💿 👘	>	ତ୍ ପ୍	$\mathbb{X} \mid \mathbb{X} \mid \mathbf{C}$	∋ Q ≚	≑ +	•	1	*	C 0	0 D	>>
₱ Designer Assistance available Run Block Automation					processin	g system7	0					
processing_system	Run Block Automation Automatically make connections in your design by checking the boxes of the its configuration options on the right.	he blocks to connect. Select a block on the left to display		AN AVI CRO			FD	DDR +		FI	DR XED_K)
- M_AXI_GP0_ACLK ZYNQ	Q ₹ ♦ ✓ All Automation (1 out of 1 selected) This option sets the bo properties will be overv ✓ ₹ ₱ processing_system7_0 This option sets the bo properties will be overv ✓ ₹ ₱ processing_system7_0 NOTE: Apply Board Pre this box, if you wish to r Instance: /processing_ Options Options	board preset on the Processing System. All current written by the board preset. This action cannot be undone. on applies current board preset and generates external D_IO, Trigger and DDR interfaces. reset will discard existing IP configuration - please uncheck o retain previous configuration. g_system7_0		M_AXI_GP0_	ZYNQ7 Prod	NQ.	M_AJ FC FCLK_R stem	XI_GP0 + CLK_CLK0 RESET0_N				
	Make Interface Externa <u>Q</u> ross Trigger In: Cross <u>T</u> rigger Out	nal: FDXED_IO, DDR Disable v Disable v OK Cancel										

Run Block Automation → FIXED_IO, DDR 연결 ACLK(AXI CLK)과 FCLK(Fabric CLK, PS→PL)을 연결



HDL Wrapper

🚴 zynq_tutorial - [C:/work/23_workp	lace/zynq_tutorial/zynq_tutoria	l.xpr] -	Vivado 2018.2			zynq_tutorial - [C:/work/23_work]	place/zynq_tutorial/zy	rnq_tutorial.xpr] - Vivado 2018.2				
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	 Simulation Sources (sim 1 (1) 	_	View Instantiation Template		processing_system7_0	Open Block Design	> 🖾 simulation	Launch the selected synthesis or implementation	i runs.)10clo225-1		
IP INTEGRATOR Create Block Design	Hierarchy IP Sources		Generate Output Products	A Croate	HDI Wranner X	Generate Block Design	Hierarchy IP			m_wrapper		
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Generate Block Design	Source File Properties		Replace File	You car you woi	i either add or copy the HDL wrapper file to the project. Use copy option if 🛛 🔒 🔒	* SIMULATION		Options		a		
Senerale Break Beeligh	🚠 system.bd		Copy File Into Project			indiaidh	System_wrapp	Launch runs on local host Number of	jobs: 8 🗸		Implementation	
	Enabled		Copy All Files Into Project	Option	15	Y RTL ANALYSIS	Enabled	Generate scripts only			Implementation	
Run Simulation	Location: Chuork	`	Enable File		Copy generated wrapper to allow user edits	> Open Elaborated Design	Location:			id	Status:	
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> Open Elaborated Design			Hierarchy Update	L		Run Synthesis					>	
-, <i>-</i>	Tcl Console × Messag	c	Refresh Hierarchy	?	OK Cancel	> Open Synthesized Design	Tcl Console N		OK Cancel		? _ 🗆 🖸	
✓ SYNTHESIS	Q ≚ ♦		IP Hierarchy				Q	1 + + + + + + + + + + + + + + + + + + +		J.		
Run Synthesis	⊖ undo	÷.,	Set as Top		em7_0/M_AXI_6P0_ACLK] [get_bd_pins processing_system7_0/FCLK_CLK0]'		Name	Constraints Status WNS TNS WHS	S THS TPWS Total Power	Failed Routes LUT	FF BRAMS URAM DSF	
> Open Synthesized Desigr	connect_bd_net [get_b		Add Module to Block Design		pd_pins processing_system7_0/FCLK_CLK0]	Run Implementation		constrs_1 Not started				
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Run Implementation	⊖ wrote : <u: 23_<="" th="" work=""><th></th><th>Set Used In</th><th></th><th>s_1/Dd/system/u1/Dd_C9545U0F.ul></th><th>Y PROGRAM AND DEBUG</th><th></th><th></th><th></th><th></th><th></th></u:>		Set Used In		s_1/Dd/system/u1/Dd_C9545U0F.ul>	Y PROGRAM AND DEBUG						
> Open Implemented Desig	<		Edit Constraints Sets		×	Senerate Bitstream						
~	Type a Tcl command here		Edit Simulation Sets			> Open Hardware Manager	<				>	
Generate HDL wrapper file and copy	into project	Ι.	Augurale EEF Files									

HDL wrapper 생성 → 블록 디자인의 HDL 인스턴스 생성 Generate Bitstream → Synthesis, Implement 거쳐 실행



PS – IMPLEMENTATION – Device





IMPLEMENTATION → Device PL 영역의 경우 사용된 영역이 없고, PS 영역만 사용됨

Export HW & Launch SDK

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ps_tutorial.sdk - C/C++ - system_wrapper_hw_platf	orm_0/system.hdf - Xilinx SDK						
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F	ОСМ
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F	SLCR Registers
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CPU:	ps7_cortexa9_0
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Board Support	Package OS
freertos10_xili standalone	nx Standalone is a simple, low-level software layer. It provides access to basic processor features such as caches, interrupts and exceptions as well as the basic features of a hosted environment, such as standard input and output, profiling, abort and exit



선택한 HW 플랫폼의 BSP 생성 BSP: 장치 드라이버, 예외 처리, 파일 및 메모리 관리

ondor various settings or y	our board support Packag	ye.		
Overview standalone drivers ps7_cortexa9_0	or Standalone_bsp_0 OS Type: standalo OS Version: 6.8 ▼	Standalone is a simple, low-level software layer. It provides access t basic processor features such as caches, interrupts and exceptions a well as the basic features of a hosted environment, such as standard input and output, profiling, abort and exit.	o as d	
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Board Support Package Settings

Control various settings of your Board Support Package.

 Overview standalone 	Configuration for OS: ps7_cortexa9_	0		
▲ drivers	Name	Value	Default	Туре
ps/_cortexa9_0	archiver	arm-none-eabi-ar	arm-none-eabi-ar	string
	compiler	arm-none-eabi-gcc	arm-none-eabi-gcc	string
	compiler_flags	-02 -c	-02 -c	string
	extra_compiler_flags	-mcpu=cortex-a9 -mfpu=vfp	-mcpu=cortex-a9 -mfpu	string
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BSP 생성 시 라이브러리 옵션, 컴파일 옵션 등 설정 가능 Default로 OK 클릭

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프로젝트 생성

- OS: standalone
- Hardware Platform
 - → Export된 HW 선택
- Target Language: C
- BSP: standalone_bsp_0
- Template: Hello World

New Project	New Project
Application Project Create a managed make application project.	Templates Create one of the available templates to generate a fully-functioning application project.
Project name: HelloWorld	Available Templates:
 ✓ Use default location Location: C:#work#10_SDx#ps_tutorial#ps_tutorial.sdk#HelloWorld Browse Choose file system: default ▼ OS Platform: standalone ▼ Target Hardware Hardware Platform: system wrapper hw platform 0 ▼ 	Dhrystone Let's say 'Hello World' in C. Empty Application Interference Hello World Interference IwIP Echo Server IwIP TCP Perf Client IwIP UDP Perf Client IwIP UDP Perf Client IwIP UDP Perf Server Memory Tests OpenAMP echo-test OpenAMP RPC Demo Openimum Peripheral Tests Peripheral Tests
Processor: ps7_cortexa9_0 Target Software Language: Q C Q C++	RSA Authentication App Zynq DRAM tests Zynq FSBL
Compiler: 32-bit Hypervisor Guest: N/A	
Board Support Package: O Create New O Use existing standalone_bsp_0	
? < Back Next > Finish Cancel	? < Back Next > Finish Cancel

HelloWorld 애플리케이션 생성

HelloWorld.c →문자열 "Hello World" 출력 #include <stdio.h>
#include "platform.h"
#include "xil_printf.h"

int main()
{
 init_platform();
}

print("Hello World\n\r");

cleanup_platform();
return 0;



D. "Hello World" 출력

PC와 보드 UART 연결 장치관리자 - 시리얼 포트(USB Serial Port) 터미널 연결

- Baud Rate: 115200
- Data Bits: 8
- Parity: None





Program FPGA

Program FPGA PL에 Bitstream 파일 다운로드

zynq_tutorial.sdk - C/C++ - system_wrapper	_hw_platforr	m_0/system.hdf - Xilinx SDK								
File Edit Navigate Search Project Run [•] • • • • • • • • • • • • • •	XIIInx W Gene Board Repo Prog Dum Prog Laun XSCT Creat	Indow Help rate linker script d Support Package Settings ositories ram FPGA pp/Restore Data_Eila Program FPGA T Console te Boot Image psr_scued_0 ps7_l2cachec_0 ps7_l2cachec_0 ps7_scued_0 ps7_afi_1 ps7_afi_1 ps7_afi_1 ps7_afi_3 ps7_afi_1 ps7_afi_3 ps7_afi_3 ps7_afi_3 ps7_afi_1 ps7_afi_0 ps7_afi_3 ps7_afi_1 ps7_afi_0 ps7_afi_1 ps7_afi_0 ps7_afi_1 ps7_afi_0 ps7_afi_1 ps7_afi_1 ps7_afi_0 ps7_afi_1 ps7_afi_0 ps7_afi_1 ps7_afi_1 ps7_afi_1 ps7_afi_1 ps7_afi_1 ps7_afi_0 ps7_afi_1 ps7_afi_1 ps7_afi_1 ps7_afi_1 ps7_afi_1 ps7_afi_1 ps7_afi_1 ps7_afi_1 ps7_afi_1 ps7_coresing_0 ps7_ocmc_0 ps7_cortexa9_1 ps7_scued_0 ps7_ocmc_0 ps7_cortexa9_1 ps7_scued_0 ps7_octexa9_1 ps7_scued_0 ps7_octexa9_1 ps7_scued_0 ps7_octexa9_1 ps7_scued_0 ps7_octexa9_1 ps7_scued_0 ps7_octexa9_0 Overview	pro-study pro-st	Connection: Device: Bitstream: Program FPGA Hardware Platform: Connection: Device: Bitstream: Partial Bitstream BMM/MMI File: Software Configural Processor	n and the ELF files tion system_wrapper_t Local Auto Detect system_wrapper.b	that reside in BRAM memo that reside in BRAM memo tw_platform_0	y Q Select Br Search Br Block RAM		Quick	Access P C
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Human Intelliger

애플리케이션 실행

Run As Launch On Hardware 애플리케이션 실행

디버그 모드 시 Debug As 실행

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🔮 ps7_in	è	Import			ps7_afi	1.00.a									
lia ps7_in	2	Export)	ps7_afi	1.00.a									
is ps7_in is ps7_in		Build Project		1	ps7_afi	1.00.a									
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ps7_in		Refresh	F5	alumei_o	ps7_globaldiner ps7 afi	1.00.a									
system 📄 system		Close Project	15	s	ps7_dma	1.00.a									
		Close Project		:_0	ps7_xadc	1.00.a									
		close officiated Projects		bus_config_0	ps7_iop_bus_cor	nfig 1.00.a						E			
		Build Configurations	+	0	ps7_ddr	1.00.a									
		Run As Fige 1 Launch on Hardware (System Debugger)													
		Debug As	۱.	2 Start Pe	erformance Analy	sis									
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		Restore from Local History	store from Local History			4 Launch on Hardware (GDB)									
		C/C++ Ruild Settings	5 Local C/C++ Application												
	83	Congrata Linker Script		Pup Con	figurations										
	<u>198</u>	Change Referenced RCD		Kull Colli	igurations							Ŧ			
		Create Root Image													
Target Conne		Create boot image		ns 🔀 🧔 Tas	ks 📃 Console	Propertie	s 📮 SDK Te	rminal 📟		📗 SDK Log 🔀				🖪 🖪 -	•
Hardware		ream						\bigtriangledown	10:05:35 INFO : Registering of			ommand handlers for SDK TCF servi			
😕 Linux TCF		Configure							10:05:35 INFO	: Launching >	SCT	T server: xsct.bat -interactive C			
QEMU Ict		Properties	Alt+Enter	n	^		Resource	Path		10:05:35 INFO 10:05:35 INFO	: Successfull	nas y do	one setting XSCT serv	/. er connec	ti
l	-		P 1 10	os (1 item)						10:05:36 INFO	: Successfull	ý do	one setting SDK works	bace ,	
										10:05:36 INFO	: Processing	comm	nand line option -hws	bec C:/wo	ork
															_
							_			•	11				•
									-						



시리얼 터미널 출력 "Hello World"

컴파일 → 실행파일(elf) 생성 프로세서, 주변장치 및 DDR3 메모리 초기화 (0x0010_0000 - 3FFF_FFFF) 애플리케이션 실행



Version: 6.7



애플리케이션 디버그

```
#include <stdio.h>
#include "platform.h"
#include "xil_printf.h"

int main()
{
    init_platform();
    while(1){
        for(int i = 0; i < 1000000; i++);
        print("Hello World\n\r");
    }
    cleanup_platform();
    return 0;
}</pre>
```

```
종료되지 않게 소스코드 수정
```

디버그 모드로 실행

Edit Navigate	Search Project Run Xilinx Wi	ndow Help	6	┩╺╡ <u>᠕</u> ╡╚╸Ҩ╸╸ ⇨ ╺
Project Explorer & Project Explorer & Projec	New Go Into Open in New Window Copy Paste Delete Source Move Rename Import Export Build Project Clean Project Refresh Close Project Close Unrelated Projects Build Configurations Run As	Ctrl+C Ctrl+V Delete F2		<pre>system.hdf system.mss helloworld.c to helloworld.c to helloworld.c: simple test application * * helloworld.c: simple test application * * This application configures UART 16550 to * PS7 UART (Zyng) is not initialized by this * bootrom/bsp configures it to baud rate 115 *</pre>
	Debug As	•	£	1 Launch on Hardware (System Debugger)
	Compare With Restore from Local History C/C++ Build Settings Generate Linker Script Change Referenced BSP	•		2 Start Performance Analysis 3 Launch on Hardware (System Debugger on QEMU) 4 Launch on Hardware (GDB) 5 Local C/C++ Application Debug Configurations

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애플리케이션 디버그



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Zynq SoC 설계





2. S/W & H/W Co-Design Tutorial

- A. AXI-4 Protocol IP 생성
 - 7-Segment \rightarrow Write Transaction
 - DIP SW \rightarrow Read Transaction
- B. PS 설정(MIO/AXI Interface/DDR Controller)
- C. PS-PL 연결(Block Design)
- D. PS Application → AXI-4 Peripheral IP 제어(Read/Write)





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AXI-4 Read/Write



전체 시스템 구성

PL

- AXI4 Slave IP
 - DIP 스위치 (Read)
 - 7-Segment(Write)

- AXI Interconnect

- M_AXI_GP[0]
- AXI4 Slave IP

PS

- M_AXI_GP[0]





시스템 블록 디자인



DATA 설정 값 COM 설정 값 순 숫자 DIG DIG DIG DIG \mathcal{A} DP A. \mathbf{E} E \mathbf{F} C D. G. 2 1 З. 0. 1 1 0 \cap n. \cap O. 0. 1 1 2 1 0 1 1 1 1. Ω 1 Ο. 1 0. 3 1 1 1 1 0 Ω. 1 0. 1 1 Ω 0. 1 1 0 1 1 1 0 1 0. 1

7-Segment 입력된 데이터를 표시

순차적으로 출력 $(DIG 1 \rightarrow 2 \rightarrow 3 \rightarrow 4..)$





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t System

A. AXI-4 Protocol IP 생성(7-Segment)
AXI-4 Protocol IP 생성(7-Segment)

Create and Package New IP 실행

Create a new AXI4 peripheral →AXI4 Peripheral IP 생성

AXI4 프로토콜 스켈레톤 IP

zynq_tutorial - [C:/work/23_wo File Edit Flow Tools	rkplace/zyng_tutorial/zyng_tutorial.zyng_	
	Create and Package New IP	.it Layout 🗸
Flow Navigator	Create Interface Definition	? ×
✓ PROJECT MANAGER	Enable Partial Reconfiguration ? _	? 🗆 🖒 X
 Settings Add Sources Language Template PIP Catalog IP INTEGRATOR Create Block Desig Onen Block Desig	Run Tcl Script Create and Package New IP X Property Editor Associate ELE File Create Peripheral, Package IP or Package a Block Design Generate Memory Please select one of the following tasks. Please select one of the following tasks. Xillinx Icl Store Packaging Options Language Templa Package your current project	Î
Generate Block Des	Settings Use the project as the source for creating a new IP Definition. Package a block design from the current project Choose a block design as the source for creating a new IP Definition.	
✓ SIMULATION Run Simulation	Image: Select a block design: system Loca Package a specified directory Choose a directory as the source for creating a new IP Definition.	Status: Messages:
 RTL ANALYSIS > Open Elaborated Design 	Gene Create AXI4 Peripheral	Active run:
 SYNTHESIS Run Synthesis 	Tcl Cc Create a new AXI4 peripheral Create an AXI4 IP, driver, software test application, IP Integrator AXI4 VIP simulation and debug demonstration design.	? _ 🗆 🗹
 Open Synthesized Design IMPLEMENTATION 	NA Sack Next> Einish Cancel	Defaults (Vivado S tation Defaults (Viva
 Run Implementation Open Implemented Designation 	n	>
Package your project and addition	al files to reuse as a piece of IP	



AXI-4 Protocol IP 생성(7-Segment)

인터페이스 설정

- Type: AXI4-Lite

- Mode: Slave

AXI 인터페이스 Skeleton IP 생성됨 - Edit-IP 실행→수정

Id Interfaces d AXI4 interfaces supported by you	ur peripheral			4		Create Peripheral Ferphieral Generation Gummary 1. IP (xilinx.com:user.fnd:1.0) with 1 interface(s)
Enable Interrupt Support	+ - Interfaces ⊕ S00_AXI	Name Interface Type Interface Mode Data Width (Bits) Memory Size (Bytes) Number of Registers	S00_AXI Lite Slave 32 64 4	 ✓ ✓		2. Driver(v1_00_a) and testapp more info 3. AXI4 VIP Simulation demonstration design more info 4. AXI4 Debug Hardware Simulation demonstration design more info Peripheral created will be available in the catalog : C:/work/23_workplace/zynq_tutorial//ip_repo Next Steps: Add IP to the repository Edit IP Verify Peripheral IP using AXI4 VIP Verify peripheral IP using JTAG interface
<	>				EXILINX.	Click Finish to continue
2		Pack Novts	Finich	Canaal		<back next=""> Finish Cancel</back>





IP Packer 프로젝트 생성됨 AXI4-Slave Skeleton IP 생성됨

AXI 인터페이스 모듈 내부에 7-Segment IP를 넣고 연결





AXI 인터페이스 모듈

데이터 Width: 32bit 데이터 레지스터 수: 4

fnd_v_1_0_S00_AXI.v

- AXI 인터페이스 모듈
- read/write 위한 hand shake
- write enable시 address에 해당하는 register에 data write

// Width of S_AXI data bus
parameter integer C_S_AXI_DATA_WIDTH = 32,
// Width of S_AXI address bus
parameter integer C_S_AXI_ADDR_WIDTH = 4

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AXI-4 Protocol IP 생성(7-Segment)





7-Segment를 작동하는 소스코드를 추가한다. seg_top.v, hex2seg.v, seven_seg.v

hex2seg.v

```
module hex2seg(
    input [3:0] hex,
    output reg [7:0] seg_data
);
```

입력된 Hex값을 Segment data로 변환하는 모듈

always @ (*) begin case(hex)

- 4'd0 : seg_data <= 8'b11111100 ; //0
- 4'd1 : seg_data <= 8'b01100000 ; //1
- 4'd2 : seg_data <= 8'b11011010 ; //2
- 4'd3 : seg_data <= 8'b11110010 ; //3
- 4'd4 : seg_data <= 8'b01100110 ; //4
- 4'd5 : seg_data <= 8'b10110110 ; //5
- 4'd6 : seg_data <= 8'b10111110 ; //6
- 4'd7 : seg_data <= 8'b11100100 ; //7
- 4'd8 : seg_data <= 8'b11111110 ; //8
- 4'd9 : seg_data <= 8'b11110110 ; //9
- 4'd10 : seg_data <= 8'b00000010 ; //-

default : seg_data <= 8'b00111010;</pre>

endcase



seven_seg.v

module seven_seg(input clk_in, input reset_n, input [31:0] data, output reg [7:0] segout, output reg [7:0] segcom); wire [7:0] seg1; wire [7:0] seg2; wire [7:0] seg3; wire [7:0] seg4; wire [7:0] seg5; wire [7:0] seg6; wire [7:0] seg7; wire [7:0] seg8; reg[15:0] clk_cnt; reg[2:0] com_cnt; hex2seg hex2seg_1 (.hex(data[31:28]), .seg_data(seg1)); hex2seg hex2seg_2 (.hex(data[27:24]), .seg_data(seg2)); hex2seg hex2seg_3 (.hex(data[23:20]), .seg_data(seg3)); hex2seg hex2seg_4 (.hex(data[19:16]), .seg_data(seg4)); hex2seg hex2seg_5 (.hex(data[15:12]), .seg_data(seg5)); hex2seg hex2seg_6 (.hex(data[11:8]), .seg_data(seg6)); hex2seg hex2seg_7 (.hex(data[7:4]), .seg_data(seg7)); hex2seg hex2seg_8 (.hex(data[3:0]), .seg_data(seg8));

```
always @ (negedge reset_n or posedge clk_in) begin
   if (!reset_n) begin
        clk_cnt <= 16'd0;
        com_cnt <= 3'd0;</pre>
    end
    else begin
        if (clk_cnt == 16'd32768)
            begin
                clk_cnt <= 16'd0;
                if (com_cnt == 3'd7) com_cnt <= 3'd0;
                else com_cnt <= com_cnt + 3'd1;</pre>
            end
        else begin
            clk_cnt <= clk_cnt + 16'd1;</pre>
        end
    end
```

end

입력된 Data값 Segment값으로 변경 클럭 입력을 분주

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8개의 7-segment를 번갈아 동작

always @ (*) begin case (com_cnt) 3'd0: begin segcom = 8'b10000000; segout = ~seg1; end 3'd1: begin segcom = 8'b01000000; segout = ~seg2; end 3'd2: begin segcom = 8'b00100000; segout = ~seg3; end 3'd3: begin segcom = 8'b000100000; segout = ~seg4; end

endmodule

end

endcase

```
segcom = 8 b00000010;
segout = ~seg7; end
default: begin
  segcom = 8 b00000001;
  segout = ~seg8; end
```

н

```
segcom = 8'b00000100;
segout = ~seg6; end
3'd6: begin
segcom = 8'b00000010;
```

```
segcom = 8'b00001000;
segout = ~seg5; end
3'd5: begin
segcom = 8'b00000100;
```

3'd4: begin

seven_seg.v

seg_top.v

외부 입력/출력 연결

```
module seg_top(
    input clk_in,
    input reset_n,
    input [31:0] data,
    output [7:0] segout,
    output [7:0] segcom
```

```
);
```

seven_seg seven_seg_u (
 .clk_in(clk_in),
 .reset_n(reset_n),
 .data(data),
 .segout(segout),
 .segcom(segcom)
);

endmodule



AXI 인터페이스 모듈 수정



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AXI 인터페이스 모듈 수정

AXI 인터페이스 모듈 fnd_v1_0_S00_AXI.v

7-Segment 모듈 선언 출력 포트 선언

AXI Interface의 slv_reg0와 7-Segment 연결

// Users to add ports here output wire [7:0] segout, output wire [7:0] segcom, // User ports ends

401 // Add user logic here seg_top seg_top_inst(

17

18 19

20 🕀

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.clk_in(S_AXI_ACLK), .reset_n(S_AXI_ARESETN), .data(siv_regO), .segout(segout), .segcom(segcom)):

// User logic ends

//AXI CLK //AXI Negative Reset //Slave Register O



FND AXI IP 탑 모듈 수정

FND AXI IP 최상위 모듈 fnd_v1_0.v

인터페이스 모듈에서 선언된 포트 선언, 외부 연결

	1
L 17.	1
	1
1.0	1
1 IŬ.	1
	1
10	1
13	1
20	Ξ

// Users to add ports here
output wire [7:0] segout,
output wire [7:0] segcom,
// User ports ends





Ргоје	ct Summary × Packa	ge IP - fnd × fnd_v1_0_S00_AXI.v	x fnd_v1_0.v x	Project Summary × Packa	age IP - fnd × fnd_v1_0_S00_AXLv × fnd_v1_0.v ×
				Packaging Steps	Review and Package
Pac	kaging Steps	File Groups		 Identification 	IP has been modified.
~	Identification	Merge changes from File G	Froups Wizard	 Compatibility 	Summary
		Q X ♦ 🖬 +	C	✓ File Groups	Display name: fnd_v1.0
~	Compatibility	Project Summary × Package IP - fm	d × fnd_v1_0_S00_AXI.v	× fnd_v1_0.v ×	otion: My new AXI IP
	File Groups				rectory: c:/work/23_workplace/ip_repo/fnd_1.0
		Packaging Steps	Customization Parameters		acing
	Customization Paramete		Marga changes from Custor	mization Parameters Wize	
	Ports and Interfaces	 Identification 	Werge changes from Custon	mization Parameters wiza	chive will not be generated. Use the settings link below to change your preference
-	r ons and intenaces	Compatibility	ୟ ≚ ≑ ୟ +	C	ackaging settings
~	Addressing and Memory	Compatibility	Nama	Description	
-		 File Groups 	Name	Description	
	a i i i ann		Customization Parameter	s	Re-Package IP
		Customization Parameters	C_S00_AXI_DATA_WIE	OTH Width of S_AXI d	ata bus
		Ports and Interfaces	C_S00_AXI_ADDR_WI	DTH Width of S_AXI a	ddress bus
			C_S00_AXI_BASEADD	R	
		 Addressing and Memory 	C_S00_AXI_HIGHADD	R	

IP 수정을 완료한 뒤, 변경 내역을 반영한다.



7-Segment IP

IP Packer로 생성한 IP Block Design에서 검색하여 추가 및 연결 가능

필요시 IP Packer로 IP 수정



A. AXI-4 Protocol IP 생성(DIP SW)

DIP_SW

외부 스위치 8bit 입력





PS에서 AXI Read Transacation으로 Data Read



AXI-4 Protocol IP 생성(DIP SW)

Create and Package New IP 실행

Create a new AXI4 peripheral →AXI4 Peripheral IP 생성

AXI4 프로토콜 스켈레톤 IP

Eile Edit Flow Tool	s Rep <u>o</u> rts	Window Layout View Help Q- Q- Q- Window Windo	rite_bitstream Complete
e 4 4 6 🔽	Create and	Package New IP	Default Layout 🗸 🗸
Flow Navigator	Create Inte	rface Definition	?
Y PROJECT MANAGER	Enable Par	tial Reconfiguration	
Settings Add Sources Language Template IP Catalog IP INTEGRATOR Create Block Design Open Block Design	Run Tcl Sci Property Ec Associate B Generate M Compile Si Xilinx Icl St Custom Cc Language S Settings	Project Summary Create and Package New IP Create Peripheral, Package IP or Package a Block Design Please select one of the following tasks. Please select one of the following tasks. Packaging Options Package your current project Use the project as the source for creating a new IP Definition. Database a block design the summary project	
Generate Block Des		A sys Package a block design from the current project Choose a block design as the source for creating a new IP Definition. Select a block design: system Package a specified directory Choose a directory as the source for creating a new IP Definition	Implementation Status:
 RTL ANALYSIS Open Elaborated Desig 	n	Gene Create AXI4 Peripheral	Active run:
 SYNTHESIS Run Synthesis Occur Outbooks 		TCI Co Create a new AXI4 peripheral Create an AXI4 IP, driver, software test application, IP Integrator AXI4 VIP simulation and debug demonstration design. THS	? _ □ [
 Open Synthesized Desi IMPLEMENTATION 	yn	NA (?) (Seate Seate Seat	Defaults (Vivado tation Defaults (V
 Run Implementation Open Implemented Des 	sign	11/19/18 4:56 PM 00:00:42	

AXI-4 Protocol IP 생성(DIP SW)

인터페이스 설정

- Type: AXI4-Lite

- Mode: Slave

AXI 인터페이스 Skeleton IP 생성됨 - Edit-IP 실행→수정

 Enable Interrupt Support Interfaces Interface Type Interface Mode Slave Data Width (Bits) 32 Memory Size (Bytes) Memory Size (Bytes) Interface Type Interface Type Interface Type Interface Mode Slave Interface Mode Slave Slave<th>I Interfaces AXI4 interfaces supported by you</th><th>ur peripheral</th><th></th><th></th><th>4</th><th>HLx Editions</th><th>Create Peripheral representation Generation Gummary 1. IP (xilinx.com:user.fnd:1.0) with 1 interface(s)</th>	I Interfaces AXI4 interfaces supported by you	ur peripheral			4	HLx Editions	Create Peripheral representation Generation Gummary 1. IP (xilinx.com:user.fnd:1.0) with 1 interface(s)
Click Finish to continue	Enable Interrupt Support	+ - Interface	AXI Name Interface Type Interface Type Interface Mode Data Width (Bits) Memory Size (Bytes) Number of Registers	S00_AXI Lite Slave 32 64 4	 ♥ ♥		2. Driver(v1_00_a) and testapp more info 3. AXI4 VIP Simulation demonstration design more info 4. AXI4 Debug Hardware Simulation demonstration design more info Peripheral created will be available in the catalog: C:/work/23_workplace/zynq_tutorial/./lip_repo Next Steps: Add IP to the repository Edit IP Verify Peripheral IP using AXI4 VIP Verify peripheral IP using JTAG interface
		>				E XILINX.	Click Finish to continue



AXI 인터페이스 모듈

IP Packer 프로젝트 생성됨 AXI4-Slave Skeleton IP 생성됨

u_sonic_v_1_0_S00_AXI.v

- AXI 인터페이스 모듈
- read/write 위한 hand shake
- read enable시 address에 해당하 는 register의 data를 출력



AXI 인터페이스 모듈 수정

AXI 인터페이스 모듈 u_sonic_v1_0_S00_AXI.v

외부 DIP SW 입력 선언

0번 Reading Register에 연결

17	// Users to add ports here
18 ;	input wire [7∶0] DIP_SW,
19 뒂 👘	// User ports ends







AXI 탑 모듈 u_sonic_v1_0.v

인터페이스에서 선언한 포트 선언 및 외부 연결

17	// Users to add ports here
18	input wire [7:0] DIP_SW,
19 👳	// User ports ends

47	dip_sw_v1_0_SOO_AXI # (
48 🕴	.C_S_AXI_DATA_WIDTH(C_SOO_AXI_DATA_WIDTH),
49	.C_S_AXI_ADDR_WIDTH(C_SOO_AXI_ADDR_WIDTH)
50)
51	.DIP_SW(DIP_SW),
52	.S_AXI_ACLK(sOD_axi_aclk),
53	.S_AXI_ARESETN(sOO_axi_aresetn),
54	.S_AXI_AWADDR(s00_axi_awaddr),
55 ¦	.S_AXI_AWPROT(sOO_axi_awprot),

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Ргоје	ct Summary × Packa	ge IP - fnd × fnd_v1_0_S00_AXI.v	× fnd_v1_0.v ×	Project Summary × Packag	e IP - fnd × fnd_v1_0_S00_AXI.v × fnd_v1_0.v ×
				Packaging Steps	Review and Package
Pac	kaging Steps	File Groups		 Identification 	IP has been modified.
~	Identification	Merge changes from File G	roups Wizard	 Compatibility 	Summary
		Q, X ♦ 🖪 🕂	C	✓ File Groups	Display name: fnd_v1.0
1	Compatibility	Project Summary × Package IP - fn	d × fnd_v1_0_S00_AXI.v ;	x fnd_v1_0.v x	ption: My new AXI IP
	File Groups				rectory: c://work/23_workpiace//p_repo/md_1.0
		Packaging Steps	Customization Parameters		aging
	Customization Paramete	 Identification 	Merge changes from Custon	nization Parameters Wiza	d chive will not be generated. Use the settings link below to change your preference
- -	Ports and Interfaces		Q 꽃 ♦ 백 +	C	ct will be removed after completion
~	Addressing and Memory	 Compatibility 	Norma	Description	
		 File Groups 	Name	Description	
	0 I I I I OII		Customization Parameters	s	Re-Package IP
		Customization Parameters	🔅 C_S00_AXI_DATA_WIE	TH Width of S_AXI da	ta bus
		Ports and Interfaces	C_S00_AXI_ADDR_WI	DTH Width of S_AXI ad	dress bus
			C_S00_AXI_BASEADD	R	
		 Addressing and Memory 	🔅 C_S00_AXI_HIGHADD	R	

IP 수정을 완료한 뒤, 변경 내역을 반영한다.



2. S/W & H/W Co-Design Tutorial

- A. AXI-4 Protocol IP 생성
 - 7-Segment → Write Transaction
 - U-Sonic → Read Transaction



- B. PS 설정(MIO/AXI Interface/DDR Controller)
- C. PS PL 연결(Block Design)
- D. PS Application > AXI-4 Peripheral IP 제어(Read/Write)



B. Processing System 설정



블록 디자인 생성



Zynq PS IP 추가



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Processing System 설정

Diagram × A	ddress Editor 🗙	? 🗆
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🗯 Designer Assi	istance available. Run Block Automation	
	processing system7 0	
	M_AXI_GP0_ACLK ZYNO	
	ZYNQ7 Processing System	

Zynq PS 설정

- I/O Peripheral \rightarrow UART
- Memory Controller
- 32b GP AXI Master





B. Processing System 설정

Documentation 🏟 Pres	ets 🔚 IP Location 🔅 Impo	ort XPS Settings					
Page Navigator —	MIO Configuration					Sum	mary Report
ynq Block Design	Bank 0 I/O Voltage LVCMC	9S 3.3V 🗸	Bank 1 I/O Voltage	EVCMOS 3.3V	7		
S-PL Configuration	← Q ¥ ≑ •	€ 0					
eripheral I/O Pins	Search: Q-						
IIO Configuration	Peripheral	ю	Signal	Ю Туре	Speed	Pullup	Direction
_	✓ I/O Peripherals						
lock Configuration	> ENET 0						
DR Configuration	> 🗌 ENET 1						
	USB 0						
MC Timing Calculation	USB 1						
iterrupts	> 🗌 SD 0						
	> 🗌 SD 1						
	> UART 0						
	> 🗹 UART 1	MIO 48 49	~				
	12C 0						
	🗌 I2C 1						
	> 🗌 SPI 0						
	> SPI 1						



UART1을 Enable 하며, MIO 48-49번 핀 할당

DRAM Controller의 값을 변경한다 (다음 페이지 표 참조)



age Navigator —	DDR Configuration		Summary Report				
nq Block Design	Prable DDR						
-PL Configuration	← Q ≍ ≑						
ripheral I/O Pins	Search: Q-						
Configuration	Name	Select	Description				
ooningaraaon	 DDR Controller Configuration 		<u>^</u>				
ock Configuration	Memory Type	DDR 3 🗸 🗸	Type of memory interface. Refer to UG585 Zynq Technical Reference				
R Configuration	Memory Part	MT41J256M16 R 🗸	Memory component part number. For unlisted parts choose "Custon				
	Effective DRAM Bus Width	MT41J128M16 HA-187E	width of DDR interface, not including ECC data width. Refer to l				
C Timing Calculation	ECC	MT41J512M8 RA-15E	es error correction code support. ECC is supported only for an				
errupts	Burst Length	MT41K128M16 HA-15E	um number of data beats the controller should use when com				
	DDR	MT41K256M16 RE-125	try clock frequency. The allowed freq range is (200,000000): 53				
	Internal Vref		Enables internal voltage reference source. Disable to use external V				
	Juntion Temperature (C)		ted operating temperature range. Controls the DDR refresh inte				
	Memory Bart Configuration	MT41K256M8 DA-15E					
		MT41K256M8 HX-15E					
	 Training/Board Details 	MT41J256M16 RE-125					
	> DRAM Training	Custom	~				

ZYNQ7 Processing System (5.5)											
Documentation 🔅 Presets 🔚 IP Location 🔅 Import XPS Settings											
Page Navigator —	DDR Configuration Summary Report										
Zynq Block Design	Enable DDR										
PS-PL Configuration											
Peripheral I/O Pins	Search: Q-										
MIO Configuration	Name	Select		Description							
Clock Configuration	DRAM Training DQS to Clock Delay (ns)										
- DDR Configuration	DQS0	0.171	8	DQS to Clock delay [0] (ns). The DQS path delay subtracted from the							
DDR Conliguration	DQS1	0.172	8	DQS to Clock delay [1] (ns). The DQS path delay subtracted from the							
SMC Timing Calculation	DQS2	0.168	8	DQS to Clock delay [2] (ns). The DQS path delay subtracted from the							
Interrupts	DQS3	0.118	8	DQS to Clock delay [3] (ns). The DQS path delay subtracted from the							
	 Board Delay (ns) 										
	DQ[7:0]	0.333	\otimes	Board delay [0] (ns). The midrange of data (DDR_DQ, DDR_DM) trac							
	DQ[15:8]	0.334	\otimes	Board delay [1] (ns). The midrange of data (DDR_DQ, DDR_DM) trac							
	DQ[23:16]	0.346	8	Board delay [2] (ns). The midrange of data (DDR_DQ, DDR_DM) trac							
	DQ[31:24]	0.358	⊗	Board delay [3] (ns). The midrange of data (DDR_DQ, DDR_DM) trac							
	Additive Latency (cycles)	0	8	Additive Latency (cycles). Increases the efficiency of the command an							
	Enable Advanced entions	\cap		Epoble Advanced DDP OoS cottings							

B. Processing System 설정

📐 Re-customize IP

7VNO7 Dressesing Cystem /F 6

B. Processing System 설정

[표] Memory 설정 내용

항목		내용	항목		내용	
Memo	ry Type	DDR3		DQS0	0.171	
Memory Part		MT41J256M 16 RE-125	DQS to Clock	DQS1	0.172	
Interr	nal Vref	Check	Delay (ns)	DQS2	0.168	
DDAM	Write leveling	Check		DQS3	0.118	
DRAM Tusining	Read gate	Check		DQ[7:0]	0.333	
Training	Read data eye	Check	Board Delay	DQ[15:8]	0.334	
			(ns)	DQ[23:16]	0.346	
				DQ[31:24]	0.358	

HUINS

Processing System 설정

Diagram \times	Address Editor 🗙		2013			Diagr	am ;	× Addre	ess Edito	or x								? 🗆	Ľ
0. Q X	$C \mid M \mid \ominus \mid Q \mid \texttt{M} \mid \neq \mid + \mid \circ_{M} \mid$	» 🗹 🖈 C 🔮	[: »			Đ,	Q,	≈ 100	Φ	Q,	* 4	+	\square_{η_i}	P 🛛	8 🖈	C	의 1	₽	>>
 Q S <i>★</i> Designer As 	Sistance available Run Block Automation processing_system - M_AXI_GP0_ACLK ZYNQ7 Processing S	Image: Constraint of the second se	Image: Second	olocks to connect. Select a block or d preset on the Processing Syster then by the board preset. This actio applies current board preset. This actio p), Trigger and DDR interfaces. et will discard existing IP configural ain previous configuration. rstem7_0	m. All current on cannot be undone. generates external ation - please uncheck	Đ	e)M_AXL4	GP0_AC	process	ing_sys YNC	atem7_	0 FIX M_AX FC FCLK_RI	DDR - ED_IO - II_GP0 - LK_CLK0 ESET0_N				_10	
		?	Options Make Interface External: <u>Q</u> ross Trigger In: Cross <u>T</u> rigger Out	FIXED_IO, DDR Disable ~ Disable ~	OK Cancel														

Run Block Automation → FIXED_IO, DDR 연결 ACLK(AXI CLK)과 FCLK(Fabric CLK, PS→PL)을 연결







시스템 블록디자인에서 생성한 AXI IP 추가

- 7-Segment
- DIP_SW

C. PS - PL 연결

Run Connection Automation 연결할 AXI IP 선택 연결

Diagram

Θ. Θ.

시스템 리셋 IP, AXI Interconnect IP 생성됨





IP의 외부 포트 우클릭 Make External 실행 포트 외부 연결

- segout
- segcom
- DIP_SW



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AXI IP Address

Base Address

DIP SW IP: 0x43C0_0000

- 0x43C0_0000 → DIP_SW
- 0x43C0_0004 → slv_reg1
- 0x43C0_0008 → slv_reg2
- 0x43C0_000C \rightarrow slv_reg3
- 7-Segment IP: 0x43C1_0000
- 0x43C1_0000 \rightarrow slv_reg0(DATA)
- 0x43C1_0000 \rightarrow slv_reg1
- 0x43C1_0000 \rightarrow slv_reg2
- 0x43C1_0000 \rightarrow slv_reg3

Diagram × Addres	s Editor 🛛 🗙				?	
Q, ¥, ♦ ₪						•
Cell	Slave Interface	Base Name	Offset Address	Range	High Address	
✓ ₱ processing_system	em7_0					
🗸 🔢 Data (32 addre	ess bits : 0x400000)00 [1G])				
∞ dip_sw_0	S00_AXI	S00_AXI_reg	0×43C0_0000	64K 👻	0x43C0_FFFF	
∞ fnd_0	S00_AXI	S00_AXI_reg	0x43C1_0000	64K 🔹	0x43C1_FFFF	

4000_0000 to 7FFF_FFF	PL	PL	General Purpose Port #0 to the PL, M_AXI_GP0
8000_0000 to BFFF_FFFF	PL	PL	General Purpose Port #1 to the PL, M_AXI_GP1



HDL Wrapper 생성

HDL wrapper 생성

- 블록 디자인의 HDL 인스턴스 생성

Event Dealon System			
Sources _X Design Sign	als	? _ 🗆 🖸	Diagram
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🗸 📄 Design Sources (1)			
∨ ●∴ system_wrapper (systen	n_wrapper.v) (1)	
> 🚵 system_i : syste	em (sv	stem.bd) (5)	rst_ps7_0_50M
🗸 🚍 Constraints	1	Source Node Prope	erties Ctrl+E
constrs_1		Open File	Alt+0
> 📄 Simulation Sources (1)		Create HDL Wrapp	er er peripheral_reset[0:0]
	-	View Instantiation T	mb_debug_sys_rst interconnect_aresetn[0:0]
		view instantiation i	- dcm locked peripheral aresetn[0:0]
		Generate Output Pr	Create HDL Wrapper
		Reset Output Produ	You can either add or copy the HDL wrapper file to the project. Use copy option if
		Replace File	you would like to modify this file.
Hierarchy IP Sources Li	t	Copy File Into Proje	i <u>i</u> •
	t -	Copy All Files Into F	Options
ource File Properties	×	Remove File from F	
evetem bd	1	Enable File	O Copy generated wrapper to allow user edits
		Disable File	● _et Vivado manage wrapper and auto-update
 Enabled 		Hierarchy Undate	
Location: C:/work/23_		Defreeb Lliesereby	
Tupo: Block Decid	6	Reliesti Hierarchy	
Block Desig		IP Hierarchy	ZYNQ/ Processing System
Part: xc7z010clg2	4	Set as Top	
Size: 58.4 KB		Add Module to Bloc	k Design

Human Intelligent System

Constraints 작성

Constraints 파일(xdc) 생성

FPGA 핀과 입출력 포트 맵핑

- 7-Segment
- DIP SW

LVCMOS 3.3V 설정

set_property PACKAGE_PIN "Y20" [get_ports "DIP_SW_0[7]"]
set_property PACKAGE_PIN "Y21" [get_ports "DIP_SW_0[6]"]
set_property PACKAGE_PIN "AB19" [get_ports "DIP_SW_0[5]"]
set_property PACKAGE_PIN "AB20" [get_ports "DIP_SW_0[4]"]
set_property PACKAGE_PIN "AA22" [get_ports "DIP_SW_0[3]"]
set_property PACKAGE_PIN "AB22" [get_ports "DIP_SW_0[2]"]
set_property PACKAGE_PIN "AA21" [get_ports "DIP_SW_0[1]"]
set_property PACKAGE_PIN "AB21" [get_ports "DIP_SW_0[0]"]
set_property IOSTANDARD "LVCMOS33" [get_ports "DIP_SW_0[*]"]

set_property PACKAGE_PIN "Y6" [get_ports "segout_0[7]"]
set_property PACKAGE_PIN "Y5" [get_ports "segout_0[6]"]
set_property PACKAGE_PIN "AA7" [get_ports "segout_0[5]"]
set_property PACKAGE_PIN "AA6" [get_ports "segout_0[4]"]
set_property PACKAGE_PIN "AB2" [get_ports "segout_0[3]"]
set_property PACKAGE_PIN "AB1" [get_ports "segout_0[2]"]
set_property PACKAGE_PIN "AB5" [get_ports "segout_0[1]"]
set_property PACKAGE_PIN "AB4" [get_ports "segout_0[0]"]
set_property IOSTANDARD "LVCMOS33" [get_ports "segout_0[*]"]

set_property PACKAGE_PIN "AB7" [get_ports "segcom_0[7]"]
set_property PACKAGE_PIN "AB6" [get_ports "segcom_0[6]"]
set_property PACKAGE_PIN "Y4" [get_ports "segcom_0[5]"]
set_property PACKAGE_PIN "AA4" [get_ports "segcom_0[4]"]
set_property PACKAGE_PIN "R6" [get_ports "segcom_0[3]"]
set_property PACKAGE_PIN "T6" [get_ports "segcom_0[2]"]
set_property PACKAGE_PIN "T4" [get_ports "segcom_0[1]"]
set_property PACKAGE_PIN "U4" [get_ports "segcom_0[0]"]
set_property IOSTANDARD "LVCMOS33" [get_ports "segcom_0[*]"]



Generate Bitstream

Generate Bitstream

- Synthesis
- Implementation
- Generate Bitstream


IMPLEMENTATION – Device

Sources	Netlist × ? _ □ Ľ	Project Summary × Device × top.xdc × system.v ×
¥ H	0	$\leftarrow \Rightarrow \bigcirc $
	 \$\[\$00_AXI_awlen (4) \$\[\$00_AXI_awsize (3) \$\[\$00_AXI_bid (12) \$\[\$00_AXI_bresp (2) \$\[\$00_AXI_rdata (32) \$\[\$00_AXI_rdata (32) \$\[\$00_AXI_rresp (2) \$\[\$00_AXI_rresp (2) \$\[\$00_AXI_wdata (32) \$\[\$00_AXI_wdata (32) \$\[\$00_AXI_wdata (32) \$\[\$00_AXI_wdata (32) \$\[\$00_aXI_wstrb (4) \$\[\$00_couplers_to_xbar_ARADDR (32) \$\[\$00_couplers_to_xbar_AWADDR (32) \$\[\$00_couplers_to_xbar_BRESP (2) \$\[\$00_couplers_to_xbar_RDATA (32) 	
Bus Net Pro	perties ? _ □ ĭ × _rdata	
Conoral	Scalar Nate	



Hardware Export & Launch SDK

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Project , 🕫 🗹 🕨 🖉 🖉 🖉 🖉 🖉 🖉 🖉 🖉 🖉 🖉 🖉 🖉 🖉	🚞 Default Layout 🗸 🗸
B Add Sources Alt+A LOCK DESIGN - system	? ×
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Close Block Design Value (system vrapper (syst	٥
Constraints (1) development tool.	t_0[*]"] ^ ?]"]
Simulgion Waveform , V © constrs_1(1) 2" [get_ports "seg_out_0[6]"] Simulgion Waveform , V © constrs_1(1)	5]"] 1"1
Checkpoint > Checkpoint > Checkpoint > Checkpoint = Check	u]"]
P → minutation sources (1) P → Export(c: a < local to Project> ✓ F: fuet, ports "seg, out 0[3]") F: fuet, ports "seg, out 0[2]") P → F: fuet, ports "seg, out 0[2]") F: f	3]"] 21"1
Text Egitor > Hierarchy P Sources Librates 3" [get_ports 'seg_out_0]1"] Text Egitor > Hierarchy P Sources Librates 3" [get_ports 'seg_out_0]1"]	1"1
Import ? OK Cancel 4" [get_ports "seg_out_0[0]"] Import }	J]"]
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Eint. Ctri+P	"] "1
Egit Export Simulation.	· · · · · · · · · · · · · · · · · · ·
	2 5 7
	(ac)
Run Implementation Run Implementation	
> Open Implemented Design	
PROGRAM AND DEBUG	
Generate Bitstream	
Voten Hardware Manager Voten Hardware Manager Voten Hardware description file for use with the SDK Launch Hardware	

Export Hardware → PS설정 정보 및 bitstream 출력 출력된 하드웨어 정보 기반으로 SDK 실행



D. PS Application(SDK)

SDK 실행 시 HDF 파일의 내용 표시

- Part name: xc7z020clg484-1
- Tool: Vivado 2018.3
- Processor Address Map
- 디자인 내 IP Block 종류
 - AXI4 Slave 인터페이스
 - FND, DIP_SW

ps_tutorial.sdk - C/C++ - system_wrapper_hw_platform_0/system.hdf - Xili

File Edit Navigate Search Project Run Xilinx Window Help

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📄 🔄 🔻 🔻 🖳 📄 system.hdf 🔀

1 - L - L

a 进 system_wrapper_hw_platform_0

b b drivers ps7_init_gpl.c

Project Explorer 😒

- 📓 ps7_init_gpl.h
- 💰 ps7_init.c 📓 ps7_init.h
- ps7_init.html
- g ps7_init.tcl

➡ Target Connections ⊠
 ▷ ➡ Hardware Server
 ▷ ➡ Linux TCF Agent

- system_wrapper.bit
- system.hdf

system_wrapper_hw_platform_0 Hardware Platform Specification

Design Information

 Target FPGA Device:
 72020

 Part:
 xc7z020clg484-1

 Created With:
 Vivado 2018.3

 Created On:
 Thu Jun 27 21:16:32 2019

Address Map for processor ps7_cortexa9_[0-1]

Cell	Base Addr	High Addr	Slave I/f	Mem/Reg
ps7_intc_dist_0	0xf8f01000	0xf8f01fff		REGISTER
ps7_scutimer_0	0xf8f00600	0xf8f0061f		REGISTER
ps7_slcr_0	0xf8000000	0xf8000fff		REGISTER
ps7_scuwdt_0	0xf8f00620	0xf8f006ff		REGISTER
ps7_l2cachec_0	0xf8f02000	0xf8f02fff		REGISTER
pc7_coup_0	0,49400000	0,49600060		DECICTED
dip_sw_0	0x43c00000	0x43c0ffff	S00_AXI	REGISTER
ps/_pmu_o	0018895000	0210093111		REGISTER
ps7_afi_1	0xf8009000	0xf8009fff		REGISTER
ps7_afi_0	0xf8008000	0xf8008fff		REGISTER
ps7_afi_3	0xf800b000	0xf800bfff		REGISTER
ps7_afi_2	0xf800a000	0xf800afff		REGISTER
ps7_globaltimer_0	0xf8f00200	0xf8f002ff		REGISTER
ps7_dma_s	0xf8003000	0xf8003fff		REGISTER
ps7_iop_bus_config_0	0xe0200000	0xe0200fff		REGISTER
ps7_xadc_0	0xf8007100	0xf8007120		REGISTER
ps7_ddr_0	0x00100000	0x3fffffff		MEMORY
ps7_ddrc_0	0xf8006000	0xf8006fff		REGISTER
ps7_ocmc_0	0xf800c000	0xf800cfff		REGISTER
ps7_pl310_0	0xf8f02000	0xf8f02fff		REGISTER
ps7_uart_1	0xe0001000	0xe0001fff		REGISTER
ps7_coresight_comp_0	0xf8800000	0xf88fffff		REGISTER
ps7_scugic_0	0xf8f00100	0xf8f001ff		REGISTER
ps7_dev_cfg_0	0xf8007000	0xf80070ff		REGISTER
ns7 dma ns	0vf8004000	0vf8004fff		REGISTER
fnd_0	0x43c10000	0x43c1ffff	S00_AXI	REGISTER
ps7_gpv_u	000000000000000000000000000000000000000	0X1891111		REGISTER
ps7_ram_1	0xffff0000	0xffffdff		MEMORY

Human Intelligent System



Create Board Support Package

BSP 생성 BSP - 장치 드라이버, 예외 처리, 파일 및 메모리 관리

SDK Z	nq_tutorial.sdk - C/C++ - system_wrapper_hw_platform_0/system	.hdf -	Xilinx SDK			
File	Edit Navigate Search Project Run Xilinx Window He	elp				
	New Alt+Shift+N ►	<u>ی</u>	Application Project			
	Open File		SPM Project			
	Open Projects from File System	Alu	Board Support Package	Dre Platform Specification		
	Close Ctrl+W	Ľ	Project	An outline is		
	Close All Ctrl+Shift+W	62	Source Folder			
	Save Ctrl+S	C	Folder			
	Save As	Ċ	Source File			
B	Save All Ctrl+Shift+S	hĭ	New Board Support	Package Project		
	Revert		Xilinx Board Suppor	t Package Project		
	Move	G	Create a Board Suppo	rt Package.		
d	Rename F2		٠			
8	Refresh F5	12.4	Project name: standa	ilone_bsp_0		
	Convert Line Delimiters To	timer	-			
8	Print Ctrl+P	0	- Use default location	un		
	Switch Workspace	0	Location. C. workwa	es_workplace#zyrid_tutorial.suk#stanualorie_osp_0		
	Restart	ichec	Choose file	system: default 💌		
R A	Import	c_0	Target Hardware			
	Export	u_0	Hardware Platform:	system_wrapper_hw_platform_0		
	Properties Alt+Enter	þ	CPU:	ps7_cortexa9_0 🔹		
	1 system.hdf [system_wrapper_hw_platf]	B	Compiler:	32-bit 👻		
	Exit	baltin	n Board Support Pack	age OS		
	psr_ur ps7_io ps7_xa ps7_dc	ma_s o_bus_ dc_0 r_0	c standalone	Standalone is a simple, low-level software layer. It provides access to basic processor features such as caches, interrupts and exceptions as well as the basic features of a hosted environment, such as standard input and output, profiling, abort and exit.		
	ps7_dc ps7_oc ps7_pi	ps/_darc_0 ps7_orer_0 ps7_pl310_0 ps7_uat 1				



Create Application

Application 프로젝트 생성

- OS: standalone
- Language: C
- BSP: standalone_bsp_0
- Template: Hello World

ps tutorial.sdk - C/C++ - standalone bsp 0/syst	tem.mss - Xilinx SDK	
ile Edit Navigate Search Project Run X	ilinx Window Help	
New	Alt+Shift+N 🕨 🍇 Application Project	
Open File	SPM Project	
Open Projects from File System	Board Support Package	
Close	New Project	Sox New Project
Close All	Application Project	Templates
Save	Create a managed make application project.	Create one of the available templates to generate a fully-functioning
Save As		application project.
Save All	Project name: sw2fnd	Available Templates:
Revert		Dhrystone Let's say 'Hello World' in C.
Move		Hello World
Rename	Location: C:#work#10_SDX#ps_tutonal#ps_tutonal.sok#sw2thd Browse	IwiP Echo Server
Refresh	Choose file system: default 💌	WIP TCP Perf Server
Convert Line Delimiters To		IwiP UDP Perf Server
Print	OS Platform: standalone	OpenAMP echo-test
Switch Workspace	Target Hardware	OpenAMP matrix multiplication Demo
Restart	Hardware Platform: system_wrapper_hw_platform_0	Peripheral Tests
Import	Processor: ps7 cortexa9 0	RSA Authentication App Zyng DRAM tests
Export		Zýný FSBL
	Transf Cafferra	
Properties		
1 system.mss [standalone_bsp_0]	Language: O C ++	
2 system.hdf [system_wrapper_hw_platf]	Compiler: 32-bit 💌	
Exit	Hypervisor Guest: N/A 👻	
	Board Support Package: Create New sw2fnd bsp	
	Qse existing standalone_bsp_0 ▼	
	(?) < <u>Back</u> <u>Next</u> > Finish Cancel	Back Next > Finish Cancel
		ļ

helloworld.c

114

```
#include <stdio.h>
#include "platform.h"
#include "xil_printf.h"
#include "xil_io.h"
#include "xparameters.h"
#include "fnd.h"
#include "dip_sw.h"
int main(){
        u8 sw_data = 0;
       u32 seg_data = 0;
        while(1){
                sw_data = (DIP_SW_mReadReg(XPAR_DIP_SW_0_S00_AXI_BASEADDR,0) & 0xFF);
                xil_printf("SW: %d\n\r", sw_data);
                seg_data = ((sw_data & 0x80) << 24)</pre>
                                  + ((sw_data & 0x40) << 20)
                                  + ((sw_data & 0x20) << 16)
                                  + ((sw_data & 0x10) << 12)
                                  + ((sw_data & 0x08) << 12)
                                  + ((sw_data & 0x04) << 8)
                                  + ((sw_data & 0x02) << 4)
                                  + (sw_data & 0x01);
                xil_printf("segdata: %u\n\r", seg_data);
                FND_mWriteReg (XPAR_FND_0_S00_AXI_BASEADDR, 0, seg_data);
                for(int i= 0; i<6000000 ; i++);</pre>
        }
```

Application 프로젝트 소스 내용 변경



Program FPGA

- PC에 보드 연결 Bitstream FPGA에 Program
- →7-Segment 초기화
 7-segment IP는 데이터 write
 현재 입력 데이터 0,
 클럭이 없어 0번 7-Segment만 켜짐



Human Intelligent System

Terminal 연결

시리얼 포트 연결

- Baud Rate: 115200
- Data Bits: 8
- Stop Bits: 1
- Parity: None
- Flow Control: None





애플리케이션 실행

Run As

→Launch on Hardware

소스코드 컴파일 시스템을 초기화 애플리케이션 탑재 후 실행

DDR3 Memory (0x0010_0000 - 3FFF_FFF)





DIP SW의 왼쪽 4비트 →상단 7-Segment DIP SW의 오른쪽 4비트 →하단 7-Segment



									165
000 63 000 31	0000 0000	000 000 000	90 90	0000 0000	0000 47 0000 15	0000 0000	00	00 10	0000 32 0101 0
ЮH	ex		Mod	Α	MC	MR	MS	M+	M-
0 D	ec ct	()	В	-	CE	с	±	√
🔘 В	in	RoL	RoR	С	7	8	9	/	%



시스템 동작 설명(Read Transaction)

sw data = (DIP SW mReadReg(XPAR DIP SW 0 S00 AXI BASEADDR,0) & 0xFF);

PS에서 Read Transaction 시 AXI_GP_Master0 – Interconnect IP 거쳐 DIP SW IP 레지스터 값 Read $0x43C0000+0 \rightarrow sw_data$ $0x43C0000+4 \rightarrow slv_reg1$ $0x43C0000+8 \rightarrow slv_reg$

ex) $sw_data = 8'b 01011100$

369 💬	always @(*)
370 🖕	begin
371	// Address decoding for reading registers
372 Θ	<pre>_case (axi_araddr[ADDR_LSB+OPT_MEM_ADDR_BITS:ADDR_LSB])</pre>
373	2'h0 : reg_data_out <= DIP_SW;
374	<pre>2 ni : reg_data_out <= siv_regi;</pre>
375	2'h2 : reg_data_out <= sIv_reg2;
376	2'h3 : reg_data_out <= sIv_reg3;
377	<pre>default : reg_data_out <= 0;</pre>
378 🏳	endcase
379 🖨	end
380 :	



시스템 동작 설명(Data Packing)

unsigned 8bit 데이터를 32bit 데이터로 패키징

- seg_data = ((sw_data & 0x80) << 24)
 + ((sw_data & 0x40) << 20)
 + ((sw_data & 0x20) << 16)
 + ((sw_data & 0x10) << 12)
 + ((sw_data & 0x08) << 12)
 + ((sw_data & 0x04) << 8)
 + ((sw_data & 0x02) << 4)</pre>
 - + (sw_data & 0x01);





시스템 동작 설명(Write Transaction)

seg_data: 32비트 packing

PS에서 Write 시 AXI_GP_Master0 -Interconnect IP 거쳐 7-Segment IP에 Write slv_reg0에 segdata 입력

slv_reg0 32비트가 7-Segment에 출력됨

FND_mWriteReg (XPAR_FND_0_S00_AXI_BASEADDR, 0, seg_data);

case (axi_awaddr[ADDR_LSB+OPT_MEM_ADDR_BITS:ADDR_LSB])

21h<mark>0</mark>:

for (byte_index = 0; byte_index <= (C_S_AXI_DATA_WIDTH/8)-1; byte_index = byte_index+1)</pre>

if (S_AX1_WSTRB[byte_index] == 1) begin

// Respective byte enables are asserted as per write strobes



Summary

FPGA IP를 AXI-4 Protocol IP로 생성할 수 있다.

- 7-Segment \rightarrow Write Transaction
- DIP-SW → Read Transaction

Vivado에서 Processing System의 설정을 할 수 있다.

- MIO/AXI Interface/DDR Controller

Block Design에서 AXI IP를 추가하여 시스템 구성을 할 수 있다.

- PS – PL 연결(Block Design)

시스템을 Export 하여 SDK에서 HW 기반의 SW를 개발할 수 있다. PS에서 AXI IP의 Read/Write Transaction을 수행할 수 있다.



References

- ZYNQ Technical Reference Guide(UG-585)
- THE ZYNQ BOOK(<u>http://www.zynqbook.com</u>)
- Vivado-Intro-FPGA-Design-HLS(UG998)

